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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,384	09/11/2003	Geum-Jong Bae	239/169 DIV	3795

7590 06/29/2005

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EXAMINER	
PHAM, HOAI V	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,384	BAE ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/08/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/274,035.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 20-21 and 24-26 are rejected under 35 U.S.C. 102(e) as being unpatentable by Ryu et al. [U.S. Pat. 6,548,862].

With respect to claims 20, Ryu discloses (fig. 13, cols. 7-10) a MOS transistor comprising:

a T-shaped gate electrode (104b and 114) disposed on a semiconductor substrate (100);

an L-shaped lower spacer (110b) covering a top surface of the semiconductor substrate (100) at both sides of the gate electrode;

a low-concentration impurity region (106) formed in the semiconductor substrate at both sides of the gate electrode (col. 8, lines 1-2);

a high-concentration impurity region (122) formed in the semiconductor substrate next to the lower spacer (col. 9, lines 49-52); and

a mid-concentration impurity region (118) disposed between the high- and low-concentration impurity regions (col. 9, lines 39-4).

With respect to claim 21, Ryu discloses that lower and upper conductive layer patterns (104b and 114) are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern so as to have an undercut region at a lower portion of the upper conductive layer pattern (see fig. 10).

With respect to claim 24, Ryu discloses that the lower conductive layer pattern (104b) is made of silicon germanium (see col. 7, lines 34-37).

With respect to claim 25, Ryu discloses that the upper conductive layer pattern (114) is made of polysilicon (see col. 8, lines 56-58).

With respect to claim 26, Ryu discloses that a surface insulating layer (110b) intervened between the gate electrode (104b and 114) and the lower spacer (110b). **Notice: as interpreting the claim in a broad scope, a surface insulating layer can also be the same as the lower spacer because the claims do not distinct the material of the lower spacer and the surface insulating layer. Therefore, the lower spacer and the surface insulating layer are considered as one layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 20-23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh et al. [U.S. Pat. 5,272,100] in view of Matsuda [U.S. Pat. 6,3166,297].

With respect to claims 20, Satoh et al. discloses (fig. 7C, cols. 5-6) a semiconductor device comprising:

a T-shaped gate electrode (3) disposed on a semiconductor substrate (1);

an L-shaped lower spacer (5) covering a top surface of the semiconductor substrate at both sides of the gate electrode (fig. 7C);

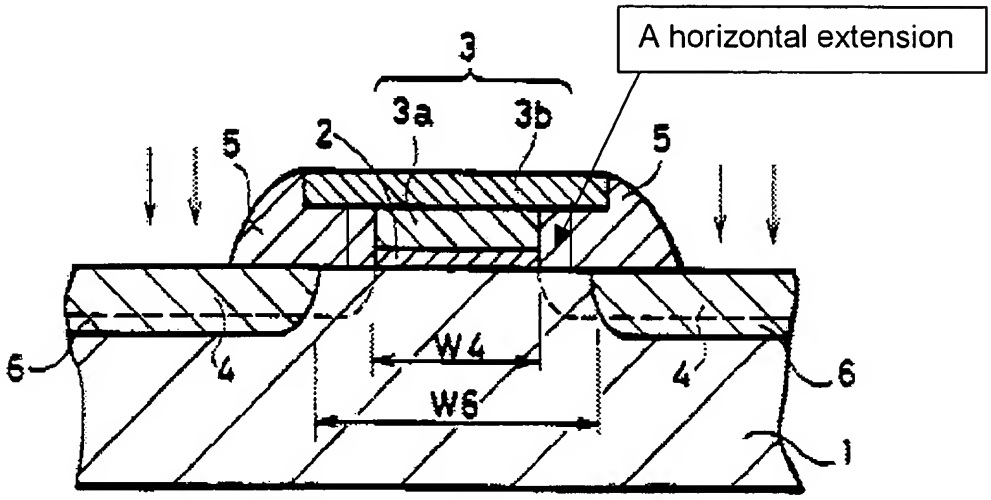
a low-concentration impurity region (4) formed in the semiconductor substrate at both sides of the gate electrode (see col. 5, lines 59-61); and

a high-concentration impurity region (6) formed in the semiconductor substrate next to the lower spacer (see col. 6, lines 28-33);

Satoh et al. fails to disclose a mid-concentration impurity region disposed between the high-and low-concentration impurity regions (6 and 4). However, Matsuda discloses that a mid-concentration impurity region (28) is disposed between the low-concentration impurity region (26) and high-concentration impurity region (34) (see fig. 3 and col. 9, lines 39-41). Therefore, it would have been obvious to one having ordinary skill in the art to modify the device of Satoh et al. by having a mid-concentration impurity region disposed between the high- and low-concentration impurity regions as taught by Matsuda in order to provide the known purpose of lower electrical field thereby improving hot carrier performance.

With respect to claim 21, Satoh et al. discloses that lower and upper conductive layer patterns (3a and 3b) are sequentially stacked, wherein the upper conductive layer pattern(3b) is wider than the lower conductive layer pattern (3a) so as to have an undercut region at a lower portion of the upper conductive layer pattern (see fig. 7C).

With respect to claim 22, Satoh et al. discloses that the L-shaped lower spacer (5) further comprises a horizontal extension filling the undercut region (fig. 7C).



With respect to claim 23, Satoh et al. discloses that the lower and upper conductive layer patterns (3a and 3b) are made of materials having an etch selectivity with respect to each other (see col. 5, lines 18-24).

With respect to claim 26, Satoh et al. discloses that a surface insulating layer (5) intervened between the gate electrode (3) and the lower spacer (5). **Notice: as interpreting the claim in a broad scope, a surface insulating layer can also be the same as the lower spacer because the claims do not distinct the material of the lower spacer and the surface insulating layer. Therefore, the lower spacer and the surface insulating layer are considered as one layer.

6. Claims 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satoh et al. [U.S. Pat. 5,272,100] in view of Matsuda [U.S. Pat. 6,3166,297] as applied to claim 21 above, and further in view of Hobbs et al. [U.S. Pat. 6,432,779].

Satoh et al. substantially discloses all the limitations as claimed above except the lower conductive layer pattern is made of silicon germanium or nitride titanium and the upper conductive layer pattern is made of polysilicon or tungsten. However, Hobbs et al. discloses that these materials, silicon germanium or nitride titanium and polysilicon or tungsten and their uses are well-known in the art for forming gate electrode (102 and 103) (see fig.4, col. 3, lines 29-33). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to select the known materials of silicon germanium or nitride titanium for the lower conductive layer pattern and polysilicon or tungsten for the upper conductive layer pattern, as taught by Hobbs et al. into the device of Satoh et al. to form the gate electrode with low resistance. Moreover, selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER